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Figure 1. Arria V GT FPGA Development Board With Two ...

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101 Innovation Drive, San Jose, CA 95134. Figure 1-2: Arria 10 GX Block Diagram FMC Altera LPC+ 9 8 X2 6 8 X8 XCVRs PCI Express 128MB FLASH X32 CPLD (FPGA) MAX V Onfig Oscillators 50M, 125M, Programmable X1 (SE) Buttons Switches LEDs X4 X8 X16 5 Micro-USB 2.0 JTAG Chain SMA CLK IN 3th, 2024

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