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Condition Mainly Used With Binary Logic Elements Where The Logic State 1 (TRUE) Is Converted To A Logic State 0 (FALSE) Or Vice Versa [IEC 60617-12, IEC 61082-2] 3.20 Logic Inversion Condition Mainly Used With Binary Logic Elements Where A Higher Physical Level Is Converted To A Lower Physical Level Or Vice Versa [2th, 2024

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DMX_Primer_rev05_WO.pdf. Starting Address When Selecting A Starting DMX Address, Always Consider The Number Of DMX Channels The Selected DMX Mode Uses. If You Choose A Starting Address That Is Too High, You Could Restrict The Access To Some Of The Product's Channels. The Geyser P5 Uses 10 DMX 4th, 2024

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