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F CLK T P 2 • The Node Transition Rate Can Be Slower Than The Clock Rate. To Better Represent This Behav Mar 4th, 2024.

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Module Full_adder_4bit(Input Cin, Input [3:0]in_a, Input [3:0]in_b, Output [3:0]sum,
Output Cout); Assign {cout,sum} = In_a + In_b + Cin; Endmodule Serial Binary
Adder: `timescale 1ns/1ps Module Serial_adder (Input Clk,reset, //clock And Reset
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