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Development Kit Note: Although The Document  
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The Next Generation SOC Processor For Emerging On-Chip ...The Processor Implements Eight Core To Provide A Total Of 64 Threads On A Die. Each Of The Core Communicates To The L2 Cache Through A Shared Memory Bus. The L2 Cache Is Divided Into 8 16 Way Set-associative 0.5MB Banks With A 64 -byte Line

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13, 2010 J. A. Abraham Verification Of SoC Designs Mar  
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Chapter 8: Single Chip And Multi-Chip Integration  
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